Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to clarify Applicants invention.

Support for the amended and new claims is found in the original claims and the Specification.

No new matter has been added.

For example support for the amendments is found in the original claims and the Specification including Figures 1D -1G, and in the Specification, e.g., at paragraph 0015:

"Yet another object of the present invention is to provide a novel MIM capacitor electrode fabrication method which improves MIM capacitor performance **by preventing plasma-induced damage to a dielectric layer during deposition of a top electrode** on the dielectric layer in fabrication of the MIM capacitor."

And at paragraph 0028:

"As shown in Figure 1D, the bottom electrode 16 is next subjected to a **thermal anneal step**. This can be carried out in a rapid thermal processing (RTP) anneal chamber or in a thermal anneal furnace using N_2 (molecular nitrogen) 18."

And at paragraph 0029:

"As shown in Figure 1E, a dielectric layer 20 is next deposited on the bottom electrode 16 and on the upper surface 12a of the substrate 12. **The dielectric layer 20 is a high-k dielectric layer** which is deposited on the bottom electrode 16 and substrate 12 according to methods which are known by those skilled in the art.The high-k dielectric layer of the fabricated MIM capacitor is preferably Al_2O_3. Other suitable dielectric materials include silicon oxide, silicon nitride, tantalum pentoxide, aluminum oxide, hafnium oxide, zirconium oxide, zirconium aluminum silicate, hafnium silicate, hafnium aluminum silicate or other dielectrics having a relatively high dielectric constant."

And at paragraph 0030:

"As shown in Figure 1F, a top electrode 22 is next deposited on the dielectric layer 20. **Preferably, the top electrode 22 is titanium nitride (TiN)**, which is deposited on the dielectric layer 20 using a gas precursor that has no organic content. The top electrode 22 is deposited on the

dielectric layer 20 using a plasma-free thermal CVD (chemical vapor deposition) process or an ALD (atomic layer deposition) process. For example, the top electrode 22 may be formed as an atomic layer deposition of titanium nitride (TiN) using $TiCl_4$ and NH_3, in which case the desired deposition product is TiN and the principle gas by-product is NH4Cl or HCl gas.

Claim Rejections under 35 USC 103

1. Claims 1-16 stand rejected under 35 USC Section 103(a) as being unpatentable over Otusuki et al. (6,919,273) taken with Olewine et al. (2003/0067023).

Otusuki et al. disclose a method for forming a TiSiN film which is used as a barrier layer and/or a capacitor electrode. The TiSiN film is taught to be made by **either a thermal CVD process or a plasma CVD process** (see Abstract; col 2, lines 13-37). Otusuki et al. also teach that **Ti and TiN films have problems as barrier layers**, especially with the use of copper and that the TiSiN **barrier** layer overcomes the problems of Ti or TiN **barrier** layers (col 1, lines 43-67).

Otusuki et al. disclose several embodiments for use of the **TiSiN barrier layer** in the formation of a capacitor (see Figures 3 through Figure 8; col 3, lines 12 - col 4, line 67; col 9, lines 30 - col 10, line 32). All the embodiments in the capacitor structure of Otusuki et al., disclose forming a **planar-type capacitor structure** over an **amorphous silicon or polysilicon plug shape** (item 51, Figures 3 and 4 ; item 61, Figures 5-9), where the amorphous silicon shape (plug) in Figure 3 and 4 form the **bottom electrode** (see col 9, lines 30-43). In the embodiments in Figures 3, a **barrier layer of SiN** is formed over the bottom electrode with a TiSiN upper electrode and in Figure 4, **a TiSiN barrier layer is formed over the bottom electrode** with a **TiSiN upper electrode**. Otusuki et al. also **teach away from using a TiN film as an upper electrode** (see col 9, lines 43-49).

In other embodiments, see Figures 5-8, a **TiSiN barrier layer (item 62) is formed over a polysilicon plug** (item 61), **except for Figure 7 where a TiSiN bottom electrode** (item 67) is **formed over the polysilicon plug.** Where a **TiSiN barrier layer is formed, it is formed under a bottom electrode made of Pt or Ru** (items 63) **or over a top electrode made of Pt or Ru** (item 68, Figure 8). In one embodiment (Figure 6), **a TiSiN upper electrode (item 66) is**

formed directly on the dielectric (item 64). Otusuki et al. also teach **that Pt or Ru are preferred as electrodes and that use of the TiSiN barrier layer protects the underlying polysilicon plug** (col 10, lines 1-15).

Nowhere do Otusuki et al. recognize or suggest a solution to the problem that Applicants have recognized and solved by their disclosed and claimed invention.

"A method of forming an MIM capacitor to prevent plasma induced damage to a capacitor dielectric"

Moreover, nowhere do Otusuki et al. disclose Applicants capacitor structure or method for forming the same including:

"providing a substrate;

providing a **capacitor opening** in said substrate;

providing a **bottom electrode in said capacitor opening;**

thermally annealing said bottom electrode;

providing a capacitor dielectric layer **in said capacitor opening on said bottom electrode;** and

depositing a top electrode on said capacitor dielectric layer **using a plasma-free deposition process.**"

On the other hand, Olewine et al. disclose a significantly different **serpentine capacitor structure** (see Figure 1) where the **bottom electrode** (see item 2, Figure 30) **is protruding above a substrate** formed from a block of conductor material such as **aluminum or copper** (see paragraph 0034) which includes an overlying conductive material (item 34) that functions as an etch stop layer **disclosed to be TiN** (paragraph 0047, 0048), a capacitor dielectric (item 36) on the TiN and an upper electrode (38) (which may be TiN) on the capacitor dielectric where the capacitor dielectric and the upper electrode are patterned **and plasma etched together** (paragraph 0036, paragraph 0070-0078) to stop on the bottom TiN layer. Olewine et al. also disclose **plasma annealing** the dielectric layer following deposition (paragraph 0062). Olewine et al. also disclose **PVD reactive sputtering to form the upper TIN electrode** (paragraph 0064).

Olewine et al. also disclose carrying out an **ammonia plasma**

treatment of the bottom electrode prior to deposition of the capacitor dielectric to remove oxidation and to inhibit formation of TiO (paragraph 0055, 0056).

Even assuming *arguendo*, a proper motivation for combining the disparate capacitor structures and processes for forming the same disclosed by Otusuki et al. and Olewine et al., such combination does not further help Examiner in producing Applicants disclosed and claimed invention or establish a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

2. Claims 17-20 stand rejected under 35 USC Section 103(a) as being unpatentable over Otusuki et al. taken with Olewine et al., above, and further in view of Iizuka (2002/0190294).

Applicants reiterate the comments made above with respect to

Otusuki et al. and Olewine et al.

The fact that Iizuka further discloses carrying out **either a plasma etchback process or a CMP process** to remove an upper portion of a bottom electrode (item 13, Fig. 7; paragraph 0087) formed in a capacitor opening after the capacitor opening has been filled with resist (item 14, Fig. 7) does not further help Examiner in making out a *prima facie* case of obviousness.

For example, Iizuka also teaches that following CMP the **resist filling the capacitor must be removed by plasma etching and that damage to the lower electrode occurs** (see paragraphs 0088, 0089). To overcome this problem, Iizuka teach forming the lower electrode, the capacitor dielectric and the upper electrode in the same ALD machine (paragraph 0090, 0100, Fig. 9I) **which is then followed** by **either a CMP process or a plasma etchback process** to remove surface portions of the capacitor structure (Fig 9J; paragraph 0112).

There appears to be no motivation to combine the teachings of the disparate capacitor structures and method for forming the same of Iizuka, Otusuki et al. and Olewine et al., which all

teach significantly different capacitor structures formed by completely different methods. For example, the capacitor structure of Iizuka when formed in the same ALD machine is never exposed to air and therefore would not need the ammonia plasma treatment in the method of Olewine et al.

Nevertheless, even assuming *arguendo*, a proper motivation for combination such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

The cited references, either alone or in combination do not produce Applicants disclosed and claimed invention and therefore fail to make out a *prima facie* case of obviousness with respect to Applicants independent and dependent claims.

The claims have been amended to clarify Applicants disclosed and claimed invention.

Based on the foregoing, Applicants respectfully submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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